The RNI-based LSPR and The IBM z14 Performance Brief

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David Hutton

STSM, IBM Z Performance and Design

hutton@us.ibm.com

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Performance is in Internal Throughput Rate (ITR) ratio based on measurements and projections using standard IBM benchmarks in a controlled environment. The actual throughput that any user will experience will vary depending upon considerations such as the amount of multiprogramming in the user's job stream, the I/O configuration, the storage configuration, and the workload processed. Therefore, no assurance can be given that an individual user will achieve throughput improvements equivalent to the performance ratios stated here.

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Topics

- Definitions: LSPR, PCI, MIPS, MSUs, RNI, CPU MF, HIS
- Fundamentals of Workload Capacity Performance
- LSPR Application-based to RNI-based Workload Evolution
- RNI Theory of Operation and Validation Analysis
- Performance Drivers with z14
- LSPR: What's new for z14
- Workload Variability
- Summary

LSPR Defined

- **Large Systems Performance Reference**
  - "Large Systems" = IBM Z
  - "Performance Reference" = expressed as generational tables of processor capacity ratios
- Natively presented as a **pricing and coarse-grain capacity planning** table
  - https://www-304.ibm.com/servers/resourcelink/lib03060.nsf/pages/lsprITRzOSv2r1?OpenDocument
- A key input to **detailed capacity planning** tooling, namely zPCR
  - Allows LPAR configuration to be input, extracts SMF (specifically CPU MF) data to identify workload characteristics and has various other knobs and switches to allow greater capacity planning precision
- The LSPR allows statements like:
  - "A high RNI workload running on a 38-way z196 (2817) is nearly throughput-wise equivalent to a z13 (2964) at a 28 way", *or ~46 z9 single-engine systems*
  - "An average RNI workload running on a 31-way zEC12 (2827) is (also) nearly throughput-wise equivalent to a z13 at a 28 way", *or ~55 z9 single-engine systems*

(System z9 2094-701 = 1.00)

Processor	#CP	PCI	MSU	Low	Average	High
2817-738	38	29124	3418	60.79	52.03	46.01
2827-731	31	30460	3571	64.90	54.41	47.53
2964-728	28	30868	3619	67.95	55.14	46.42

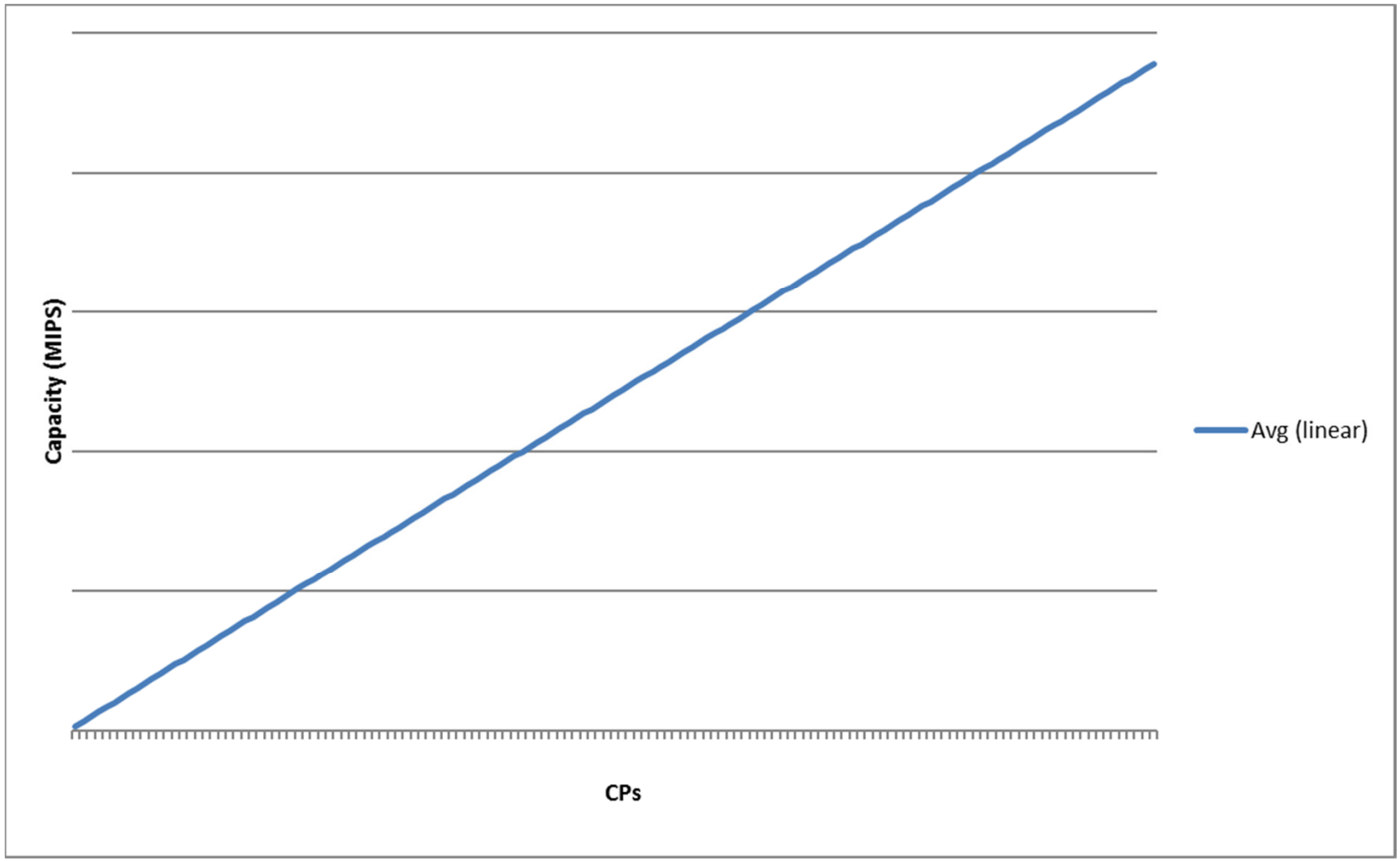
PCI and MIPS? MSUs? RNI?

- PCI – Capacity metric for HW pricing
  - Processor Capacity Index, aka “Pricing MIPS”
  - At one time rooted in “true MIPS”, or millions of instructions per second
- MSUs – Capacity metric for SW pricing
  - Millions of Service Units (per hour); rooted in SUs or “service units” used by SRM / WLM
  - On recent machines PCI / MSUs = ~8..8.5
- RNI – “Relative Nest Intensity”
  - The “Nest” is IBM Z’s custom processor-interconnect and off-core cache memory hierarchy
  - “Numeric RNI” is a formula-based metric that reflects the average storage hierarchy **depth** at which L1 misses are typically serviced for a given workload; *or a “nest depth metric”*
  - “LSPR Workload Match (or Characterization or Category)” is typically “LOW”, “AVERAGE” or “HIGH”-RNI, and is determined by a table that considers the L1MP (“L1-cache miss percentage”) and numeric RNI
    - Since z196 these three workload categories have facilitated a very good means of matching customer workload to the LSPR
    - zPCR adds finer-grain “LOW-AVERAGE” and “AVERAGE-HIGH”-RNI characterizations
  - The intention is that a workload’s RNI characteristic remains constant across machine generations – *hence “relative”*

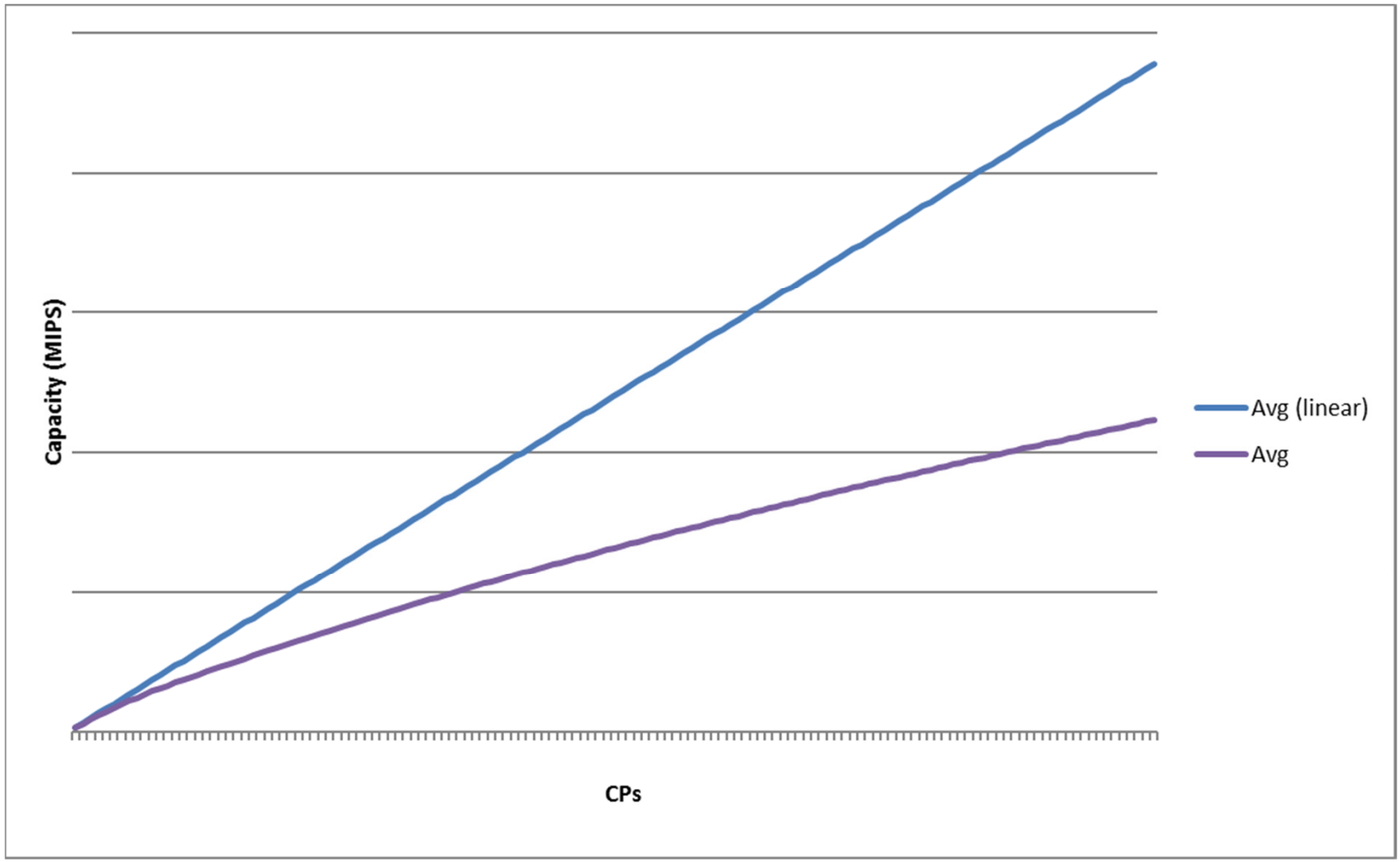
CPU MF?

- What is the Central Processing Unit Measurement Facility?
  - A facility available starting with z10 GA2 that provides processor and nest **COUNTERS**
  - Also capable of providing time-in-Csect type **SAMPLES**
  - Data gathering controlled through z/OS HIS (HW Instrumentation Services)
    - Collected on an LPAR basis
    - Written out to System Management Facility “SMF” 113 records, one per interval per logical engine in the LPAR
    - Minimal overhead
- How can the COUNTERS be used today?
  - To supplement current performance data from SMF, RMF, DB2, CICS, etc.
  - To help understand why performance may have changed
- How can the COUNTERS be used for future processor planning?
  - **They provide the data that determine LSPR RNI-based workload characterizations**
  - **zPCR can automatically process EDF files created from CPU MF data to provide an RNI-based workload match**
- Reference John Burg’s CPU MF presentation at SHARE

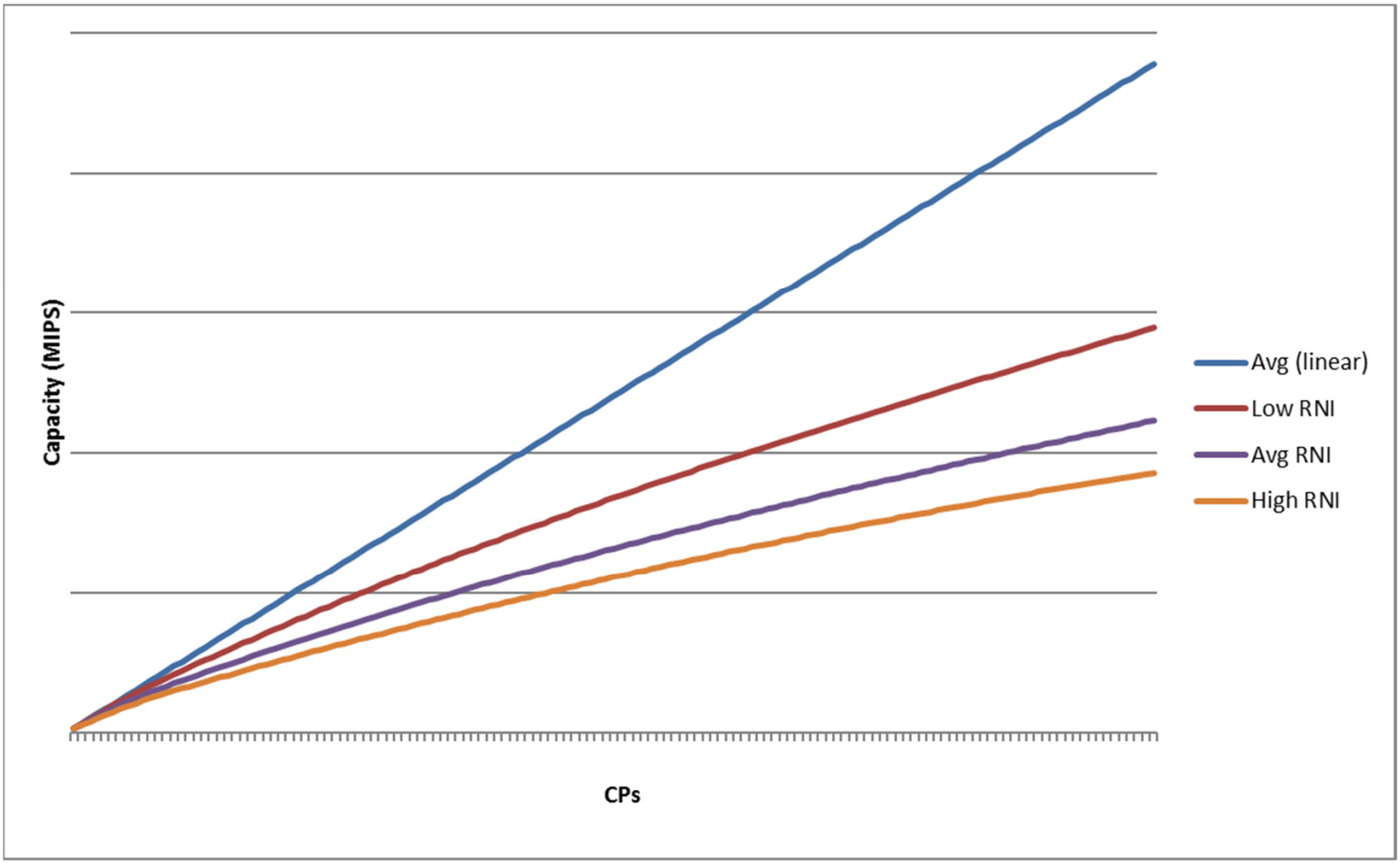
LSPR – general idea



LSPR – general idea



LSPR – general idea



How the LSPR is Created

- IBM Z provides **capacity comparisons or ratios among processor generations** based on a variety of measured workloads which are published in the **Large Systems Performance Reference (LSPR)**
  - https://www-304.ibm.com/servers/resourcelink/lib03060.nsf/pages/lsprindex
- Old and new processors are measured in the same environment with the same workloads at high utilizations - typically 90..95% busy
- Over time, workloads and environment are updated to stay current with customer profiles
  - Old processors measured with new workloads or environments may have different average capacity ratios compared to when they were originally measured
- Provides single number metrics MIPS, MSUs and SRM Constants
  - Based on the ratios for
    - The “average”-RNI workload
    - The “median” customer LPAR configuration

How the LSPR is Created: Median LPAR Configuration Profiles

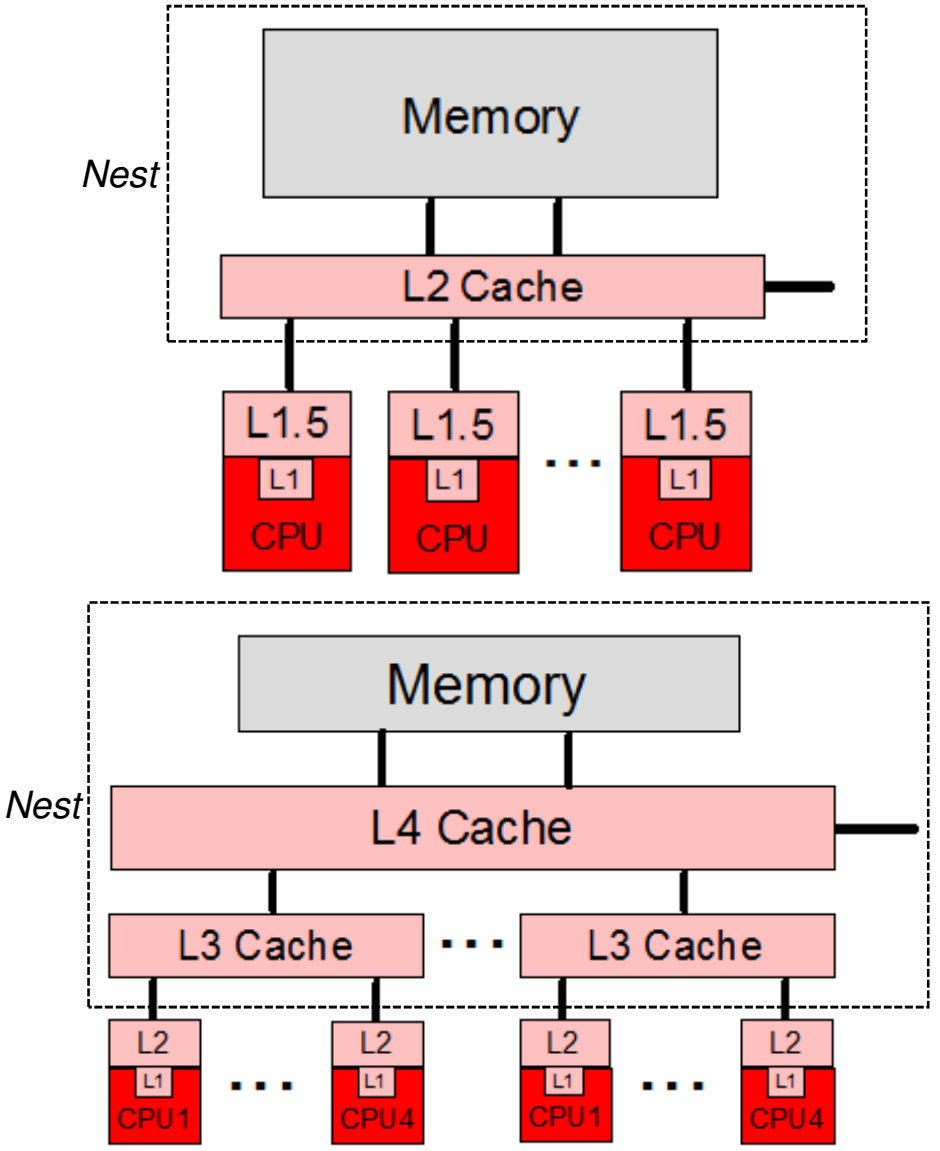
- Total number of z/OS images (or LPARs)
  - 5 images at low N-way models to 9 images at high N-ways
- Number of major images (>20% weight each)
  - 2 images across full range of models
- Size of images
  - Low to mid N-way models have at least one image close to N-way of model
  - High N-way models generally have largest image well below N-way of model
    - These models tend to be used for consolidation
- Logical to physical CP ratio
  - Low-end near 5:1
  - Most of the range 2:1
  - High-end near 1.3:1
- Book configuration
  - 1 "extra" book or drawer beyond what is needed to contain purchased CPs
- ICFs and IFLs
  - ICFs + IFLs = 3

Three Fundamental Components of Workload Capacity Performance

- **Instruction Path Length ("IPL" or processed "instruction count") for a transaction or job**
  - Application dependent, of course
  - Can also be sensitive to N-way (due to MP effects such as locking, work queue searches, etc.)
  - But generally doesn't change much on moves between processors of similar capacity and/or N-way
- **Instruction Complexity (Microprocessor design, a.k.a. "non-finite-L1-cache CPI")**
  - Many design alternatives
    - Cycle time (GHz), instruction architecture, pipeline, superscalar, Out-Of-Order, branch prediction and more
  - Workload effect
    - May be different with each processor design
    - But once established for a workload on generation of processor, it does not change very much over the N-ways
- **Outer, Shared Cache and Memory Hierarchy or "Nest" (a.k.a. "finite-L1-cache CPI")**
  - Many design alternatives
    - Cache (levels, size, private, shared, latency, protocols), controller, data busses
  - Workload effect
    - May be different with each nest design, and quite variable over the N-ways of same generation of processor
    - Sensitive to many factors: locality of reference, dispatch rate, IO rate, competition with other applications and/or LPARs, proximity to other physical engines assigned to the same LPAR (starting with z13), etc.
  - **Relative Nest Intensity: the root of the MP effect**
    - Activity beyond the private cache(s) is the most sensitive area, due to longer latencies involved
    - Reflects activity distribution and latency to chip-level caches, book (or node)-level caches and memory
    - Level 1 cache miss percentage also important
    - Data for calculation available from CPU MF (SMF 113) starting with z10 GA2

z196 vs z10 Hardware Comparison

- z10
  - CPU
    - 4.4 GHz
    - 4 cores per CP chip
  - Caches
    - L1 private 64k i, 128k d
    - L1.5 private 3 MB
    - L2 shared 48 MB per node
    - 5 CP chips per L2 per node
- z196
  - CPU
    - 5.2 GHz
    - Out-Of-Order execution
    - 4 cores (and 1 L3) per CP chip
  - Caches
    - L1 private 64k i, 128k d
    - L2 private 1.5 MB
    - L3 shared 24 MB per CP chip
    - L4 shared 192 MB per node
    - 6 CP chips per L4 per node



LSPR Application-based to RNI-based Workload Evolution (thanks CPU MF!)

- Historically, LSPR workload capacity curves (primitives and mixes) had application names or been identified by a “software” captured characteristic
  - For example, CICS, IMS, OLTP-T, CB-L, LoIO-mix, TI-mix, etc
- However, capacity performance is more closely associated with how a workload is using and interacting with a processor “hardware” design
- With the availability of CPU MF (SMF 113) data starting with z10, the ability to gain insight into the interaction of workload and hardware exists; e.g., **Cycles Per Instruction, or CPI**
- But the problem with CPI is it can vary dramatically for the same workload from machine generation to machine generation
  - **What you want is a metric that captures the major source of CPI variation *and* generally holds steady from generation to generation – *specifically something like… Relative Nest Intensity!***
- The z196 LSPR introduced three new RNI-based workload categories which replaced all prior primitives and mixes
  - **LOW, AVERAGE and HIGH RNI**
- All migrations to z196, zEC12 and z13 have validated this approach
  - Detailed study of ~20 customers times ~5 LPARs each for each of the 3 migration scenarios of z10 to z196, z196 to zEC12, and zEC12 to z13 = ~300 LPARs
- RNI-based methodology for workload matching has long since been the default in zPCR
  - *Accordingly, be sure to extract your CPU MF data per LPAR into EDFs and upload to zPCR!!*

LSPR RNI-based Workload Categories

- Categories developed to match the profile of data gathered on customer systems
  - Over 300 data points (LPARs) used in the profiling: ~20 clients, ~5 LPARs each, 3 generations of migration
  - *Consider becoming a contributor!*
- Various combinations of prior workload primitives are measured on which the new workload categories are based
  - Applications include CICS, DB2, IMS, MQ, OSAM, VSAM, WebSphere, COBOL, utilities
- LOW RNI
  - Workload curve representing light use of the memory hierarchy
  - Similar to past high N-way scaling workload primitives
- AVERAGE RNI
  - Workload curve expected to represent the majority of customer workloads
  - Similar to the past low-IO or “LoIO-mix” curve
- HIGH RNI
  - Workload curve representing heavy use of the memory hierarchy
  - Similar to the past data-intensive or “DI-mix” curve
- zPCR extends these published categories
  - LOW-AVERAGE: 50% LOW and 50% AVERAGE
  - AVERAGE-HIGH: 50% AVERAGE and 50% HIGH

General Trends of Factors that Influence Relative Nest Intensity (RNI)

Low	Relative Nest Intensity	High
Batch	Application Type	Transactional
Low	IO Rate	High
Single	Application Mix	Many
Intensive	CPU Usage	Light
Low	Dispatch Rate	High
High locality	Data Reference Pattern	Diverse
Simple	LPAR Configuration	Complex
Extensive	Software Configuration Tuning	Limited

RNI-based LSPR Workload Characterization Table

L1MP	Numeric RNI (or "Nest Depth Metric")	RNI-based LSPR Workload Characterization
< 3	>= 0.75 < 0.75	AVERAGE LOW
3 to 6	> 1.0 0.6 to 1.0 < 0.6	HIGH AVERAGE LOW
> 6	>= 0.75 < 0.75	HIGH AVERAGE

- Applies to all processors z10 and later
- Table may change based on feedback
- Reference following slide plus John Burg's CPU MF presentation at SHARE Atlanta 2016 for Numeric RNI ("Nest Depth Metric") formula details:
  - http://s23.a2zinc.net/clients/SHARE/Summer2016/Public/SessionDetails.aspx?FromPage=Sessions.aspx&SessionID=1588&SessionDateID=13

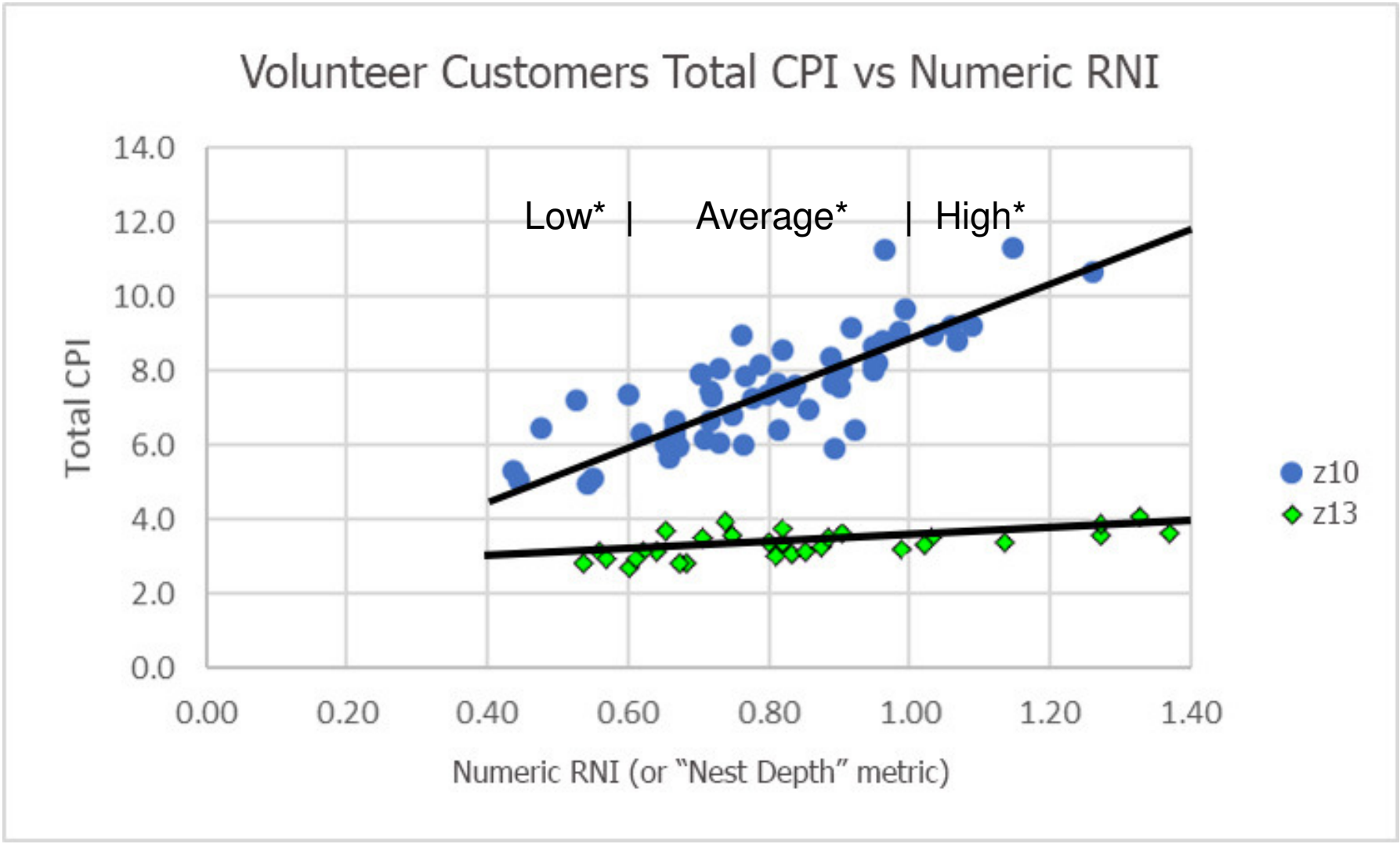
Numeric RNI ("Nest Depth Metric") Formulas Per Generation

- z10 RNI = 1.0 x (1.0xL2LP + 2.4xL2RP + 7.5xMEMP) / 100
  - L2LP: percentage of L1 misses sourced from the local book* L2 cache
  - L2RP: percentage of L1 misses sourced from a remote book* L2 cache
  - MEMP: percentage of L1 misses sourced from memory

- z196 RNI = 1.67 x (0.4xL3P + 1.0xL4LP + 2.4xL4RP + 7.5xMEMP) / 100
- zEC12 RNI = 2.3 x (0.4xL3P + 1.2xL4LP + 2.7xL4RP + 8.2xMEMP) / 100
- z13 RNI = ~~2.6~~ **2.3** x (0.4xL3P + 1.6xL4LP + 3.5xL4RP + 7.5xMEMP) / 100
  - *NOTE: updated in Feb 2017 based on client CPU MF data from migrations to z13***
- z14 RNI = 2.4 x (0.4xL3P + 1.5xL4LP + 3.2xL4RP + 7.0xMEMP) / 100
  - L3P: percentage of L1 misses sourced from the shared chip-level L3 cache
  - L4LP: percentage of L1 misses sourced from the local book/node/drawer* L4 cache
  - L4RP: percentage of L1 misses sourced from a remote book/node/drawer* L4 cache
  - MEMP: percentage of L1 misses sourced from memory

- * "book" pertains to z10, z196 and zEC12; "node" pertains to z13; "drawer" pertains to z14
- ** NOTE: these formulas may change in the future

CPU MF: Customer Workload Characterization Summary



** Assumes L1MP in 3-to-6 range*

Using zPCR vs the LSPR z/OS Tables

- For the most accurate capacity sizing ...
  - Use zPCR customized LPAR configuration planning function
    - http://www-01.ibm.com/support/docview.wss?uid=tss1prs1381
    - Should always be used for final configuration planning for any upgrade
  - **For all LPARs: 1) enable CPU MF and 2) include EDFs in the zPCR configuration!**

- LSPR tables may be used for high level capacity comparisons
  - Multi-image table represents average LPAR configuration and is the basis for all single-number metrics
  - See Gary King's **"To MIPS or Not To MIPS"** presentation at SHARE San Jose 2017 for the "gotchas" of using unadjusted LSPR-table MIPS:
    - http://events.share.org/Winter2017/Public/SessionDetails.aspx?FromPage=Sessions.aspx&SessionID=2032&SessionDateID=21

z14 Performance: Design Highlights – Primary Performance Drivers

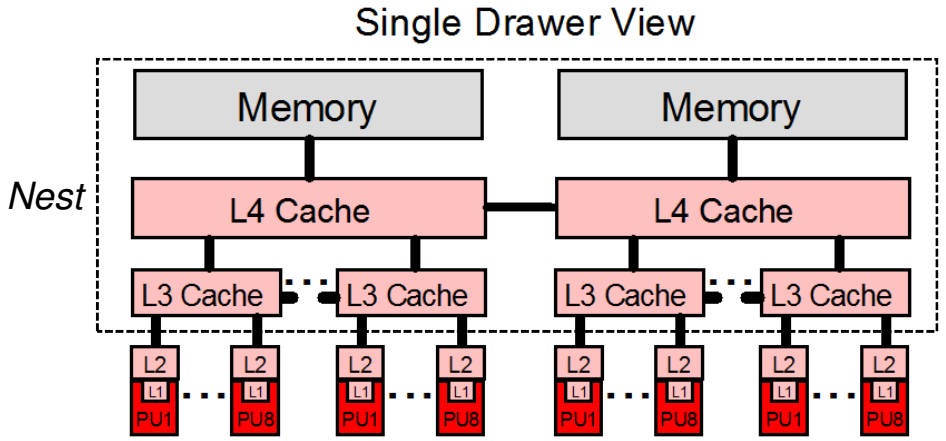
- Processor
  - Microarchitectural enhancements (branch prediction, resource turnaround, prefetching)
    - Improved IPC <-> Reduced CPI
  - Second generation SMT for zIIPs, IFLs and, new to z14, SAPs (always enabled)
    - Introduced on z13, improved on z14 – better sharing, multiple and faster translation engines
  - Second generation SIMD unit for analytics introduced on z13 – new decimal architecture introduced on z14
  - Up to 10 processor units per chip vs 8 on z13
  - Up to 170 configurable processor units per CEC on z14 vs 141 on z13
  - 4 different uni speeds (as always)
- Memory Subsystem
  - Continued focus on keeping data closer to the processor unit
    - Larger L1, L2, L3 caches. Individual L4s are larger but now shared by 2x L3s *so effectively smaller*
    - Improved IPC (Instructions Per Cycle) – aka Reduced CPI (Cycles per Instruction)
    - Second generation NUMA – reduced variability with single-node drawer
  - 3.2X configurable memory (8TBx4 drawers = **32TB on z14** vs 10TB on z13)
    - Primary use cases: supports large volume of Linux guests and in-memory analytics
    - New DB2 supports 16TB buffer pools however z/OS supports 4TB-max images; *give them a reason to grow!*
- PR/SM
  - 85 customer partitions (same as z13)
  - Improved algorithms
  - HiperDispatch
    - Exploits new chip configuration
    - Required for SMT on zIIPs

z14 Performance: Design Highlights – More Details

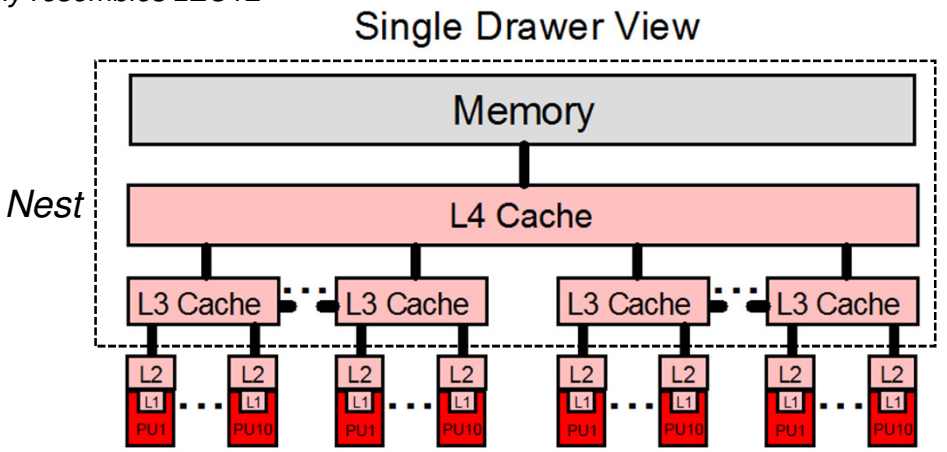
- **Processor uArch Improvements**
  - **5.2 GHz z14 vs 5.0 GHz z13 (+4%)**
  - Merged L1/TLB1 – eliminates TLB1 miss penalty, inlined TLB2 access on L1 miss mitigates TLB2 access penalty
  - Four HW-implemented translation engines on z14 vs one picocoded engine on z13
  - 2x CRSTE (combined region segment table entry) and 1.25x PTE (page table entry) growth
  - Branch prediction improvements; 33% BTB1-and-2 growth, new perceptron predictor and simple call-return stack
  - Pipeline optimization; improved instruction delivery, faster branch wakeup, reduced execution latency, improved OSC prediction, …
  - Optimized 2nd generation SMT; improved thread balancing, multiple outstanding translations, optimized hang avoidance mechanisms
  - Improved Hot Cache Line handling; dynamic throttling – e.g., “XI strong-arming” and a Hot Line Table
- **Cache Improvements**
  - L1 I-Cache increased from 96K to 128K per Core (1.33x)
  - L2 D-Cache increased from 2MB to 4MB per Core (2x)
  - L3 Cache increased from 64MB to 128MB per CP (2x)
  - L4-NIC Cache changed from 480MB+224MDir to 672MB L4, *however only one L4 per drawer on z14 vs two on z13*
  - L4 sequential prefetch
- **Storage Hierarchy Improvements**
  - Single SC Topology (Reduced system latencies)
  - Redesigned System protocols (Reduce contention points)
  - New L3 fetch miss resumption on L4 sequential pre-fetch conflict
  - Bus Feeds and Speeds
  - Wider processor store bus
  - Improved Hot Cache Line handling; contention affinity, single SC
- **Software / Firmware Improvements**
  - PR/SM: Improved Memory Affinity, improved logical partition placement algorithms based on z13 experience
  - New Translation Management Facility (avoid expensive ops)
  - New per-work-unit dispatch cache footprint metrics (cache efficiency)
  - Improved Hot Cache Line handling (new instructions)

z14 vs z13 Hardware and Topology Comparison

- z13
  - CPU
    - 5.0 GHz
    - Major pipeline enhancements
    - 1 picocoded translation engine
  - Caches
    - L1 private 96k i, 128k d
    - L2 private 2 MB i, 2 MB d
    - L3 shared 64 MB / chip
    - L4 shared 480 MB / node
      - Plus 224 MB NIC



- z14 – *L3 clustering and cache sizes aside, topology strongly resembles zEC12*
  - CPU
    - 5.2 GHz
    - Logical directory w/ inclusive TLB
    - 4 HW-implemented translation engines
  - Caches
    - L1 private 128k i, 128k d
    - L2 private 2 MB i, 4 MB d
    - L3 shared 128 MB / chip
    - L4 shared 672 MB / ~~node~~ drawer



z14 Performance: Capacity Highlights

- Full speed single-thread capacity ratios relative to z13
  - **Average 1.10x z/OS at equal Nway**; *range 1.06 to 1.17 based on workload type and Nway*
  - **Average 1.31x max box capacity**; *range 1.26 to 1.35 based on workload type*
    - 170w z14 vs 141w z13
- Subcapacity models
  - Uniprocessor capacity ratio to full speed z14

model	z13 mult	z13 MIPS	**z14 mult**	**z14 MIPS**
401	0.15	250	**0.14**	**256**
501	0.44	746	**0.41**	**751**
601	0.63	1068	**0.59**	**1081**
701	1.00	1695	**1.00**	**1832**

  - Up to 33 CPs (general purpose processors) for each subcap model; z13 had up to 30 CPs
- SMT capacity option
  - Same as z13, customers can choose to run two HW threads per core on IFLs and zIIPs
    - Controlled by OS parm at the LPAR level
    - Added HW threads appear as additional processors to the OSes
  - New to z14, SMT will additionally be employed on SAPs – not user-controllable
  - Capacity improvements per IFL and zIIP core:
    - z14 ST -> z14 SMT: 10 .. 40%, average 25%
    - z13 SMT -> z14 SMT: ~15% z/VM Guest 2, ~10% others

LSPR: What's New For z14

- Workload updates
  - Upleveled software: z/OS 2.2, DB2 11, CICS 5.3, IMS 14, WAS 8.5.5.9, COBOL 6.1
  - Minor tweaks to three (LOW, AVG and HIGH RNI) hardware-characteristic-based workload categories
    - Based on CPU MF data from customers' zEC12 to z13 migrations
- HiperDispatch continues to be turned on for all measurements
- LSPR will continue to publish only single HW thread capacity in the multi-image table
  - Multi-image (MI) table
    - Median LPAR configuration for each model based on customer profile
      - Including effect of average number of ICFs and IFLs
    - Most representative for vast majority of customers
    - Basis for single-number metrics MIPS, MSUs and SRM constants
- zPCR continues to allow any configuration to be modeled
  - Customized LPAR configurations and workloads
  - Utilizes CPU MF (SMF 113) from the EDF file to determine LSPR Workload Match (LOW, AVERAGE, and HIGH) from L1MP and numeric-RNI
  - SMT capacity effect will be included via a user controlled "dial"
    - Set dial to reflect the estimated capacity increase of two threads over one thread
    - If no SMT history, pre-install guidance is to set the dial to the default 25% across the board; previously z13 had defaults of 20% for z/VM Guest 2 and 25% for zIIPs
    - Post-install guidance in setting dial from metering data available in RMF and the z/VM Performance Report

Variability Among Workloads on z14

- Performance variability is generally related to fast clock speed and physics
  - Increasing memory hierarchy latencies relative to microprocessor speed
  - Increasing sensitivity to frequency of "missing" each level of processor cache
  - Workload characteristics – RNI in particular – are determining factor, not application type
- zEC12 demarked the end of an era while z13 ushered in a new one
  - Substantial frequency gains from generation to generation are no more
  - Greater reliance on performance driven by improved IPC in core and nest (e.g., “uarch enhancements”) vs frequency
  - Workloads do not all react the same to these changes
  - Microbenchmarks are particularly susceptible to this effect
- Moving away from the MCM to a NUMA topology also created variability
  - Greater reliance on PR/SM to do the right thing in placing LPARs
  - Enabling HiperDispatch maximizes cache reuse potential and minimizes cache line migration traffic across the topology
- z14 is a second-generation z13
  - Mitigated some of the NUMA variability by largely removing the nodal boundary within a drawer
  - More cores per drawer and each with higher capacity than z13 means more work can “fit” on a single drawer
  - Added architecture and updated z/OS to more smartly manage locks
- **We expect migrations to z14 from z13 to be stable**
- **Workloads migrating to z14 from zEC12 and prior can expect to see similar albeit slightly less variability than the typical z13 experience**

z14 Performance: Summary

- Full speed single-thread capacity ratios relative to z13
  - **Average 1.10x z/OS at equal Nway**; *range 1.06 to 1.17 based on workload type and Nway*
  - **Average 1.31x max box capacity**; *range 1.26 to 1.35 based on workload type*
- Capacity improvements per IFL and zIIP core:
  - z14 ST -> z14 SMT: 10 .. 40%, average 25%
  - z13 SMT -> z14 SMT: ~15% z/VM Guest 2, ~10% others
- 3.2X configurable memory (8TBx4 drawers = **32TB on z14** vs 10TB on z13)
  - Primary use cases: supports large volume of Linux guests and in-memory analytics
  - New DB2 supports 16TB buffer pools however z/OS supports 4TB-max images; *give them a reason to grow!*
- Optimized 2nd generation SMT
  - Improved thread balancing, multiple outstanding translations, optimized hang avoidance mechanisms
- **Variability**
  - **We expect migrations to z14 from z13 to be stable**
  - **Workloads migrating to z14 from zEC12 and prior can expect to see similar albeit slightly less variability than the typical z13 experience**

Thanks for coming! hutton@us.ibm.com